REMARKS

Claims 1-12 are pending in this application of which claims 1, 6, 7, and 8 are independent. Amendment has been made to claims 1, 2, 8, and 9. Care has been taken to avoid the introduction of new matter. Reconsideration in light of the following remarks is respectfully solicited.

The Examiner is thanked for the Examiner's interview of October 2, 2003. During the interview, claimed amendments incorporated herein were discussed. The Examiner agreed that the claim amendments distinguish from the Nagata reference, and therefore would overcome the claim rejection. Please find our remarks below.

The Examiner objects to claims 2 and 9 for minor informalities. Correction has been made to claims 2 and 9, as suggested by the Examiner. Withdrawal of the claim objection is respectfully solicited.

The Examiner maintains the rejections of claims 1-12. Namely, the Examiner rejects claims 1-6 and 8-12 under 35 U.S.C. §103(a) as being unpatentable over Nagata in view of Shimazaki, and rejects claim 7 under 35 U.S.C. §103(a) as being unpatentable over Nagata in view of Shimazaki and further in view of Mitra. The rejections are respectfully traversed.

Claims 1 and 8 have been amended to recite "representing the digital circuit . . . as a time-division group of parasitic capacitors comprising parasitic capacitors each connected between a source line and a ground line to be charged at a specific timing . . . ." Support for this claim amendment can be found in, for example, the first full paragraph from line 18 on page 13 to line 12 on page 17 of the Specification and in Figs. 2A-2C.

The Examiner's position regarding Nagata is as follows: Nagata discloses that a value for the parasitic capacitances is determined every predetermined time interval wherein

the time interval is set according to the switching operations of the logic gates. Nagata also discloses controlling switching action to charge or discharge the capacitors according to a truth table, and that a truth table is well known in the art to be a table listing of all possible combinations of inputs and the corresponding output of a Boolean function. Applicants disagree with the Examiner's characterization of Nagata relative to the claim language.

Referring to Nagata Figs. 7b and 7c, Nagata selects a state of a group of logic circuits L from a truth table for input N, which is applied to only the first logic gate L. Changing inputs to the first logic gate L affects other logic gates in this series, as outputs of each logic gate L are connected to inputs of subsequent logic gates in the series. However, for any combination of inputs N selected, Nagata fails to identify which logic gates, if any, in the series will be activated or charged. The truth table of Nagata provides of charging/discharging the parasitic capacitors at a certain instant, and does not disclose the concept of "time-division." Despite this, the Examiner states that the parasitic capacitors of Nagata may be charged in series by selecting different input condition according to the truth table; however, there is no disclosure of selecting different states or even changing states in accordance with a truth table to charge the capacitors in series, as the Examiner contends. Simply, a state is selected from the truth table. Nagata does not teach a time-division group of parasitic capacitors each connected . . . [and each capacitor] charged at a specific timing, as claim 1 recites. Accordingly, Nagata fails to disclose each and every element of claims 1, 6, 7, and 8.

Other claim distinctions are pointed out in the response of April 3, 2003, and are incorporated herein by reference. Withdrawal of the rejection of claims 1-6 and 8-12 are respectfully solicited.

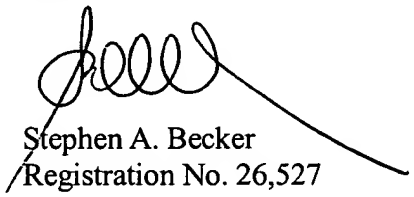
As claim 7 includes all the limitations for setting in claim 6, which in turn includes the limitations recited by claim 1, claim 7 is not obvious for the reasons discussed above. Withdrawal of the rejection is specifically solicited.

If there are any questions regarding this response or the application in general, a telephone call to the undersigned would be appreciated to expedite prosecution of this case.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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